REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 25-32 are pending for examination in this application. Claims 23 and 24 have been canceled without prejudice or disclaimer while Claims 25, 27, 29, and 31 have been amended to better clarify the nature of the carrier concentration in each current path defined between each of the main emitter(s) and each of the collector(s) having a maximum value at each opposing MOS gate side of high-resistance base layer(s), all without the introduction of any new matter. See, for example, FIGS. 46 and 47 and the corresponding description at page 72, line 21-page 74, line 6.

The outstanding Office Action presents a rejection of Claim 23 under 35 U.S.C. § 103(a) as being unpatentable over Yanagisawa et al (U.S. Patent No. 5,874,750, Yanagisawa), and a rejection of Claims 24-32 under 35 U.S.C. § 103(a) as being unpatentable over Yanagisawa in view of Takeda et al (1998 International Symposium article, Takeda).

Before considering the outstanding prior art rejections applied to Claims 23-32, it is believed that a brief summary of the invention thereof would be helpful. In this regard, the present invention involves a chip-like voltage-driven power semiconductor device that has features including:

(1) The power semiconductor device comprises a chip-like injection enhanced gate transistor (IEGT).

(2) The IEGT has a current sense emitter in addition to a main emitter.

(3) The IEGT has a current path representing a carrier concentration having a maximum value at the MOS gate side of the high-resistance (N-) base layer (see FIGS. 46 and 47 and the corresponding description of page 72, line 21 to page 74, line 6).

(4) The IEGT is mounted between plate-like collector and emitter electrodes to form a press-contacting type package.

As to feature (3), the IEGT according to the present invention represents a particular carrier concentration (accumulation) characteristic in a current path between the cathode (emitter) and the anode (collector) as shown in FIG. 47. The carrier concentration curve of the IEGT, shown by the solid line in FIG. 47, has its maximum value at the MOS gate side of the high-resistance (N-) base layer, while that of an IGBT, shown by the broken line, has the maximum value at the anode (collector) end a' and shows a low concentration value at the MOS gate side of the N– base layer thereof. In the on-state of the IEGT device, an excessive carrier accumulation occurs at the MOS gate side of the high-resistance (N-) base layer as shown in FIG. 47 so that the resistance in the MOS gate side of the high-resistance (n-) base layer becomes very low. Thus, a large current flows in the IEGT unlike the IGBT. This is what causes the electrode injection efficiency of the IEGT to be 0.73 or more which never occurs in the IGBT because, as shown in FIG. 47, the carrier concentration in the MOS gate side of the high-resistance (N-) base layer of the IGBT is too low as compared with that of the IEGT. Thus, such a large carrier concentration in the channel region does not occur in the case of the IGBT as shown in FIG. 47 and the artisan would clearly understand this.

Turning to the rejection of Claim 23 under 35 U.S.C. § 103(a) as being unpatentable over Yanagisawa, it is noted that Claims 23 and 24 have been canceled which renders this rejection and the rejection applied to Claim 24 moot.

Moreover, with regard to the rejection of Claims 25-32 under 35 U.S.C. § 103(a) as being unpatentable over Yanagisawa in view of Takeda, it is clear that Yanagisawa at best teaches an IGBT having an emitter electrode plate 16 and a collector electrode plate to form a pressure-contact type IGBT. Though Yanagisaw may show an emitter sensing electrode connected to an emitter of the IGBT, this emitter sensing electrode does not function as a current sensing terminal but functions as a voltage sensing or monitoring terminal (see column 5, lines 33-35 and column 7, lines 1-6, for example).

Also, Yanagisawa cannot provide the now claimed carrier concentration in the recited current path between the emitter(s) and collector(s) that has a maximum value at opposing MOS gate side(s) of the high-resistance base layer(s) that each of independent Claims 25, 27, 29, and 31 now recite. As this claimed carrier concentration of each of these independent claims cannot be provided by the Yanagisawa IGBT structure, there can be no reasonable conclusion reached that predicates unpatentability on the IGBT teachings and suggestions of Yanagisawa.

Furthermore, electron injection efficiency of 0.73 or more also cannot be provided by the Yanagisawa IGBT structure because the required carrier concentration cannot be achieved. Optimization of that which is impossible remains impossible and even if the artisan attempted to obtain the Claim 25 recited electron injection efficiency of 0.73 or more with the Yanagisawa IGBT structure, the attempt would fail.

Page 4 of the outstanding Action attempts to suggest that the Yanagisawa IGBT structure can be nevertheless considered to be somehow modified by emitter region doping to achieve some one or another undefined "applications of the device." This approach of assuming the existence of desirable emitter doping changes to provide totally undocumented device applications that are merely concluded assumed to be possible applications for the Yanagisawa IGBT structure clearly violates precedent that the PTO has itself indicated must be followed. See MPEP § 2143.01 (Rev 1, Feb. 2003) pointing to In re Lee, 277 F.3d 1338, 1342-44, 61 USPQ2d 1430, 1433-34 (Fed. Cir. 2002) as "discussing the importance of relying on objective evidence." With regard to this need to present objective evidence, Lee further points out (at 61 USPQ2d 1435) that "[c]onclusory statements such as those here provided do not fulfill the agency's obligation."

Takeda shows no more than a trench gate NPT-IGBT and NPT-IEGT with a low on-state voltage. Takeda does not correct for the above-noted deficiencies in Yanagisawa.

Accordingly, Claims 25-32 should be considered to be allowable over anything reasonably taught or suggested by these references taken alone or together in any proper combination based upon the arguments set forth. In addition, Claims 25-32 should be considered to be allowable over anything reasonably taught or suggested by these references taken alone or together in any proper combination because there has been no showing of an objective basis properly establishing reasonable motivation to combine teachings from these references, much less how such combined teachings would meet the limitations of these claims.

Also, it is noted that the drawings filed on December 19, 2002 have not been acknowledged. We enclose copies of the drawings filed along with a copy of the date-stamped filing receipt indicating the filing thereof and request acknowledgment thereof.

As it is believed that no other issues remain outstanding in this application, it is further believed that this application is, accordingly, in condition for formal allowance and an early and favorable action to that effect is, therefore, respectfully requested.

Respectfully submitted,

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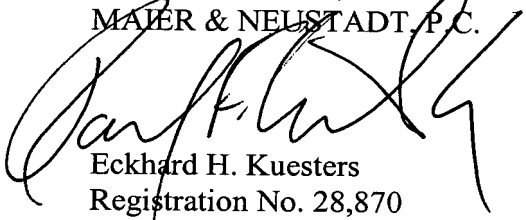

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Serial No. 09/684,904

In the matter of the Application of: Hironobu KON, et al.

For: VOLTAGE-DRIVEN POWER SEMICONDUCTOR DEVICE

Due Date: 12/19/02

The following has been received in the U.S. Patent Office on the date stamped here

- ■ RCE
- ■ Check for **$740.00**
- ■ Dep. Acct. Order Form
- ■ Amendment under 37 CFR 1.114 & 1.111 with Marked-up Copy
- ■ Letter to the Official Draftsman with 8 sheets of Formal Drawings